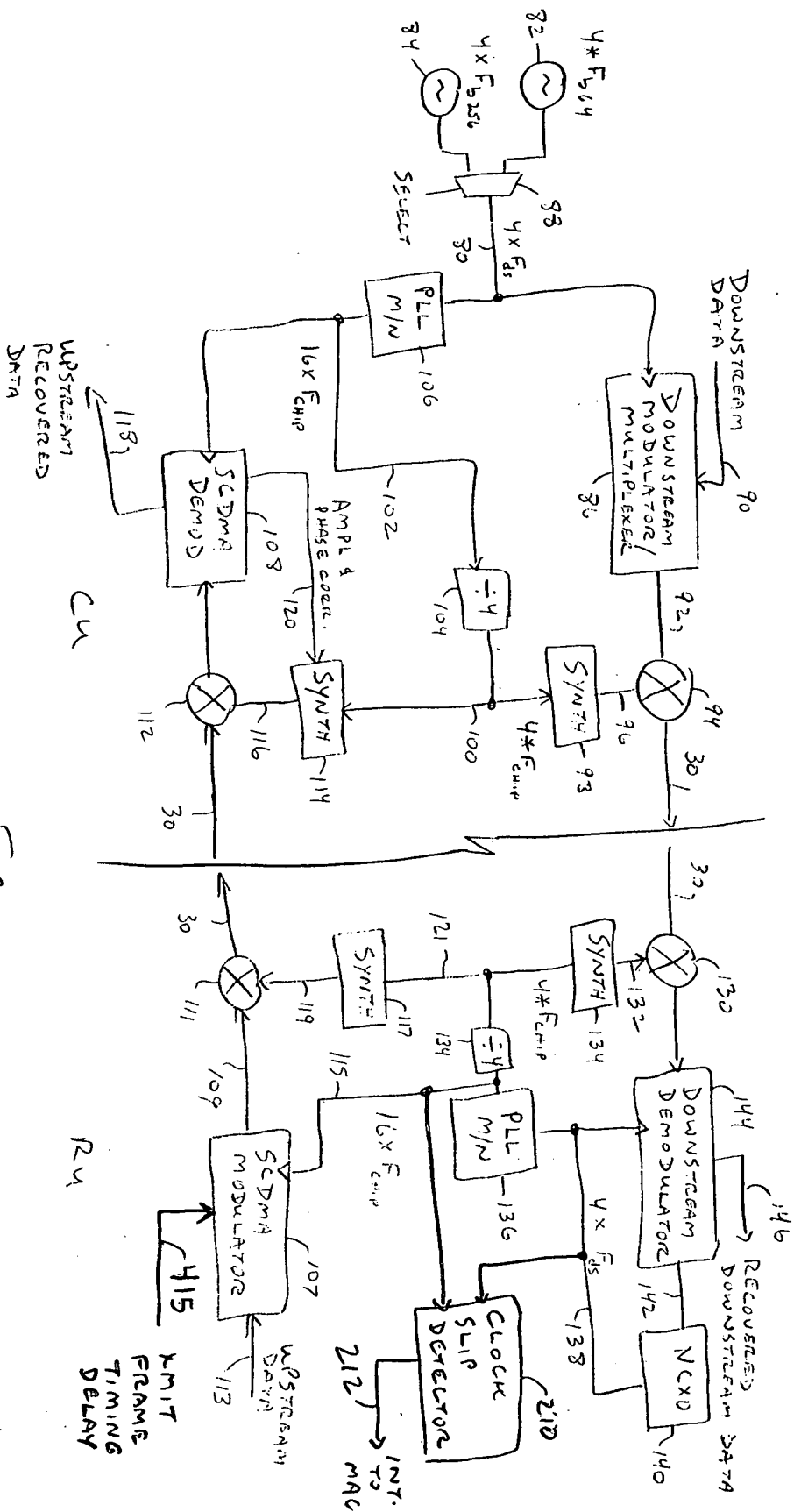


۲۷

Fig 1

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FRAME TIMING DELAY



09074036 050698

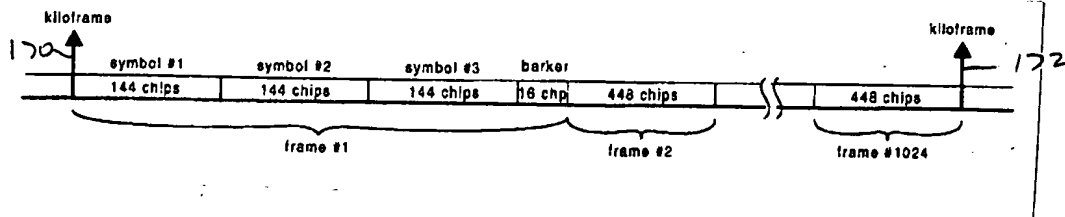


FIG. 3

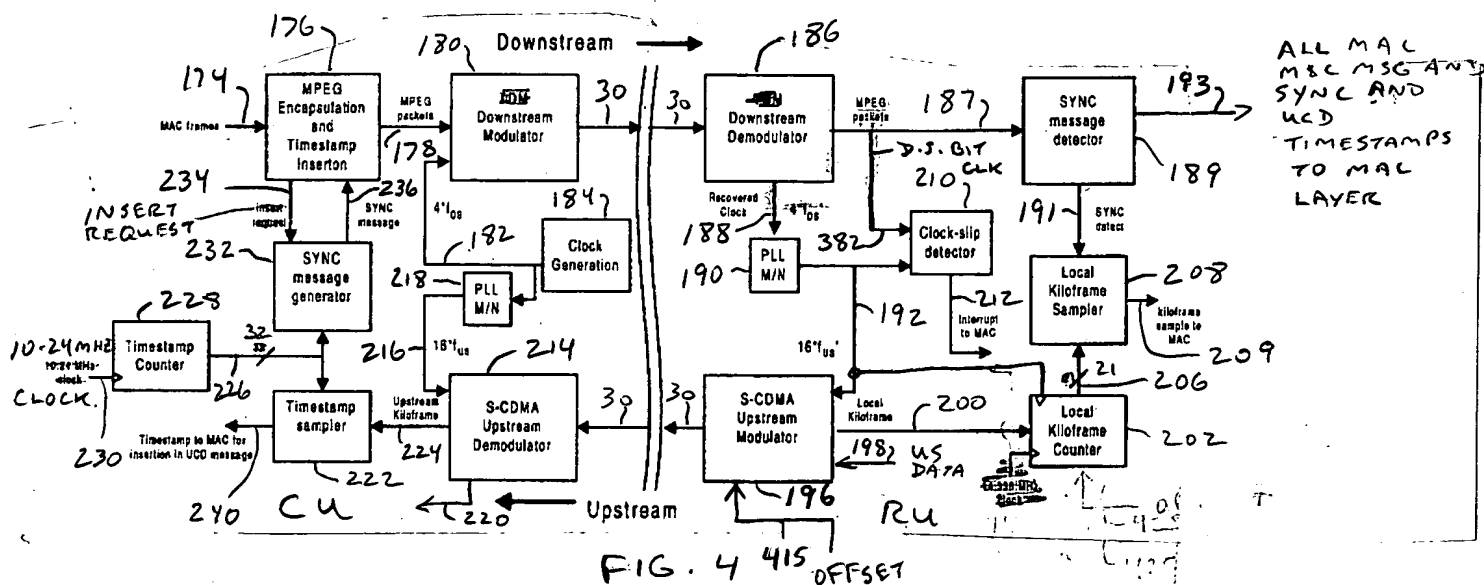
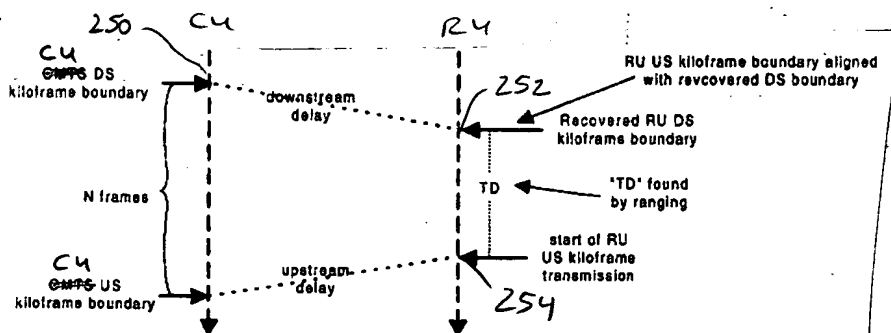


FIG. 4 415 OFFSET



SCDMA DS, SCDMA US
FIG. 5

00074036 050698

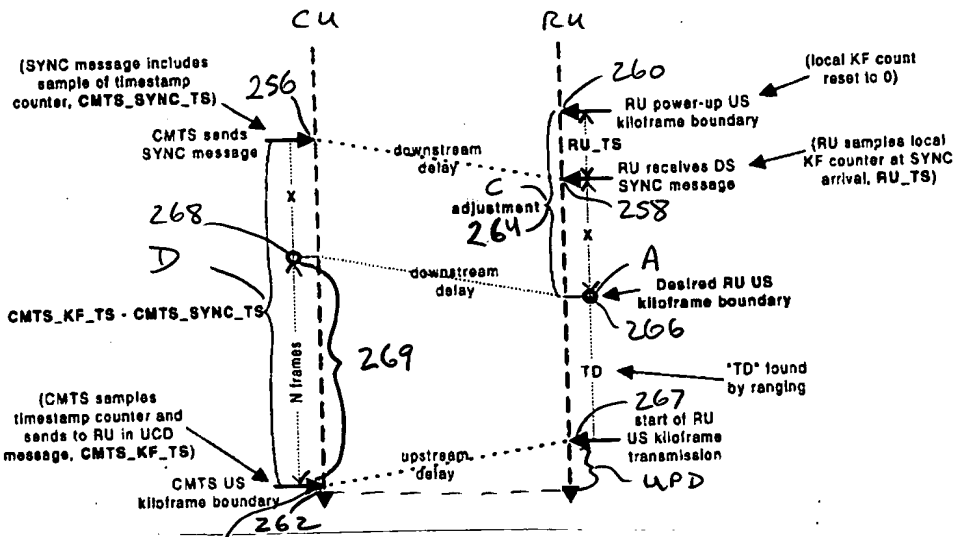


FIG. 6

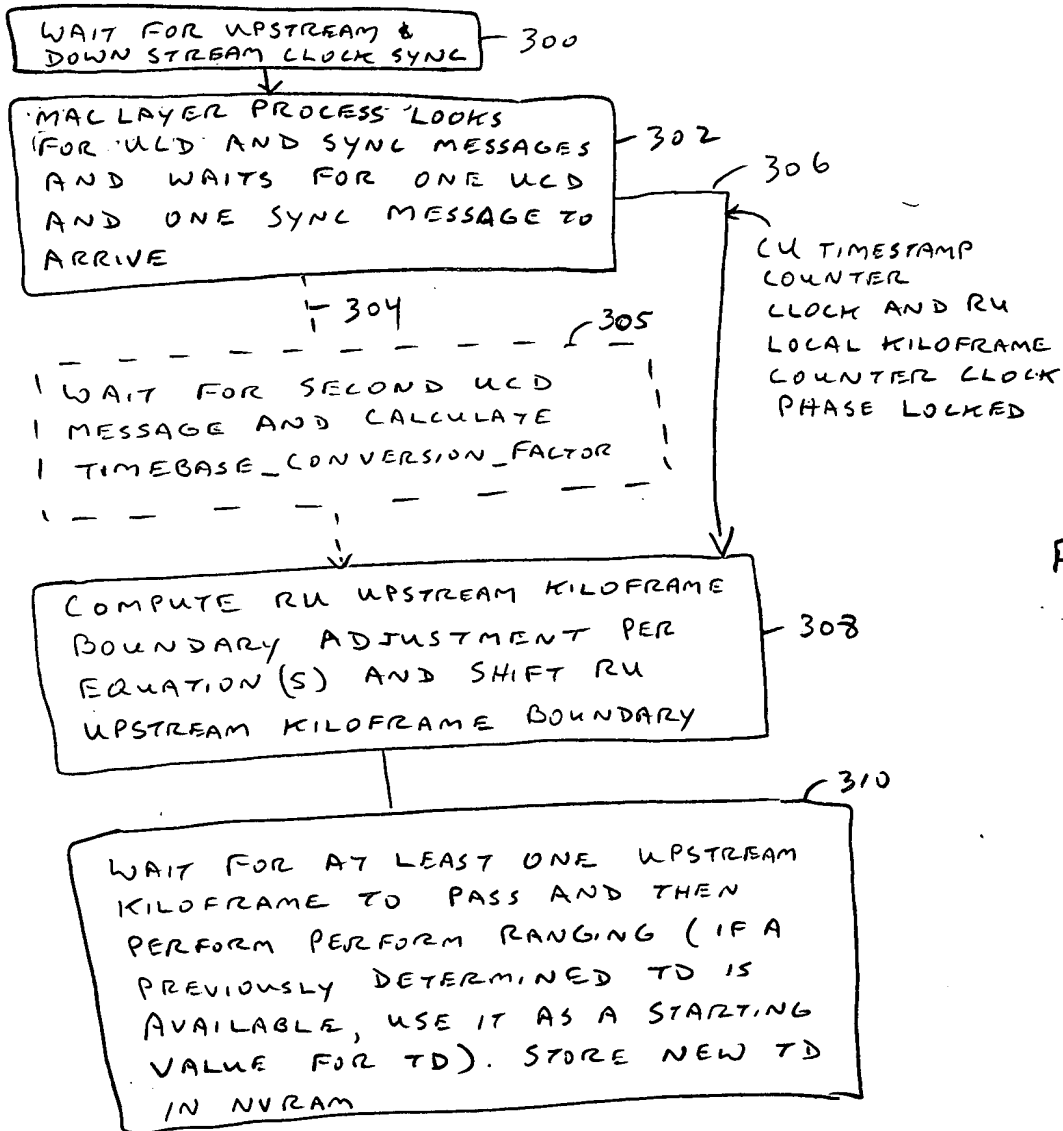


FIG. 7

2024036 050690

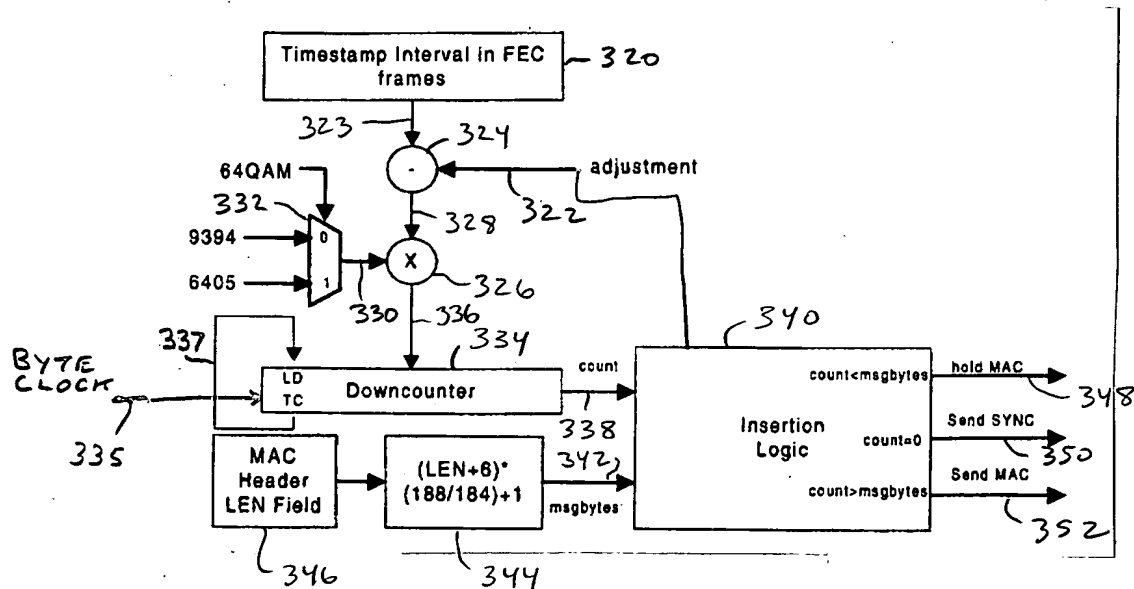


FIG. 8

Table 1 64 QAM SYNC Start Position Adjustments

SYNC Start Position in Bytes	SYNC Adjustment in FEC frames
0-5	2
155-167	4
167-183	2

FIG. 9

Table 2 256 QAM SYNC Start Position Adjustments

SYNC Start Position in Bytes	SYNC Adjustment in FEC frames
0-2	6
3-5	7
155-160	1
161-166	2
167-172	3
173-178	4
179-184	5
185-187	6

FIG. 10

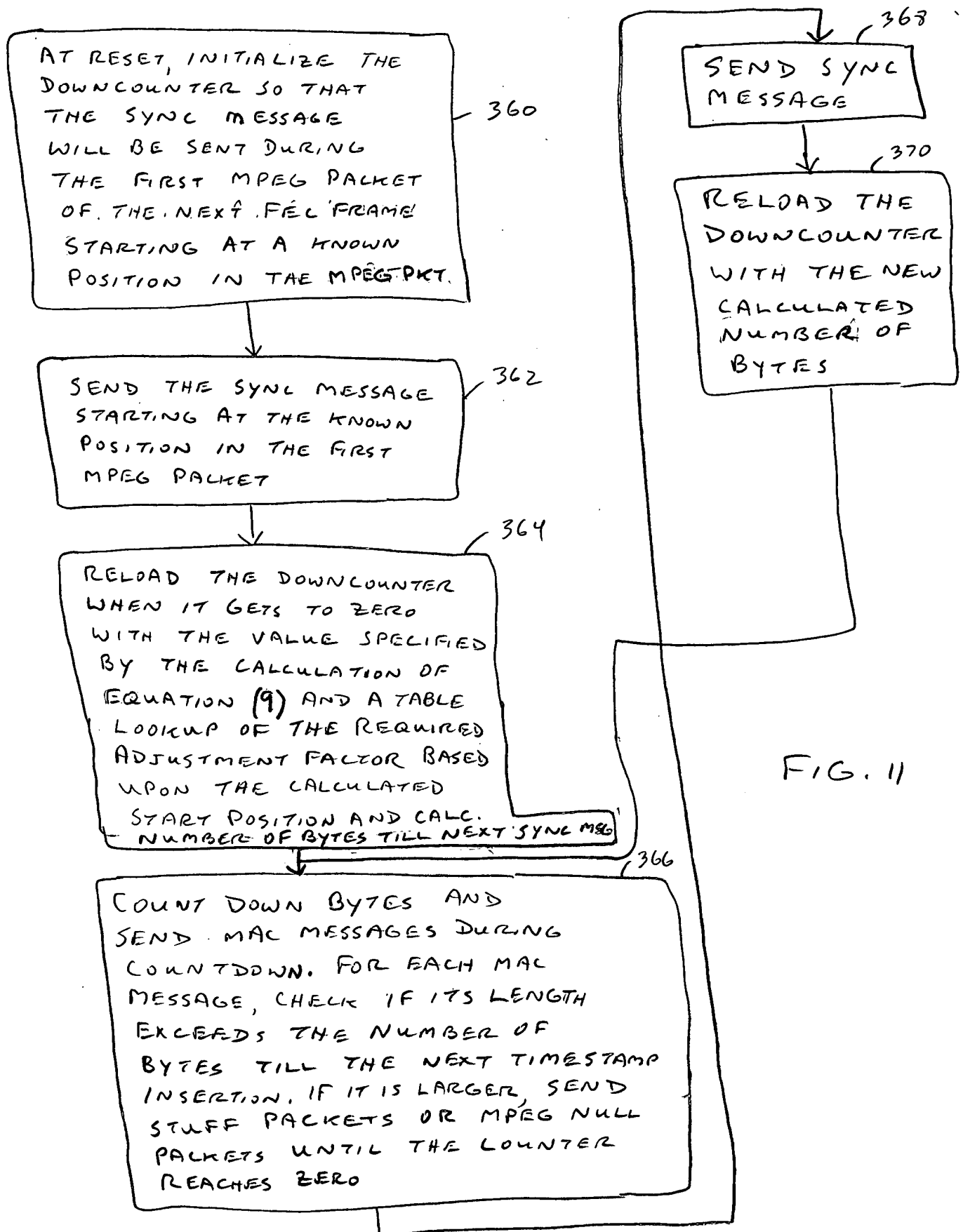


FIG. 11

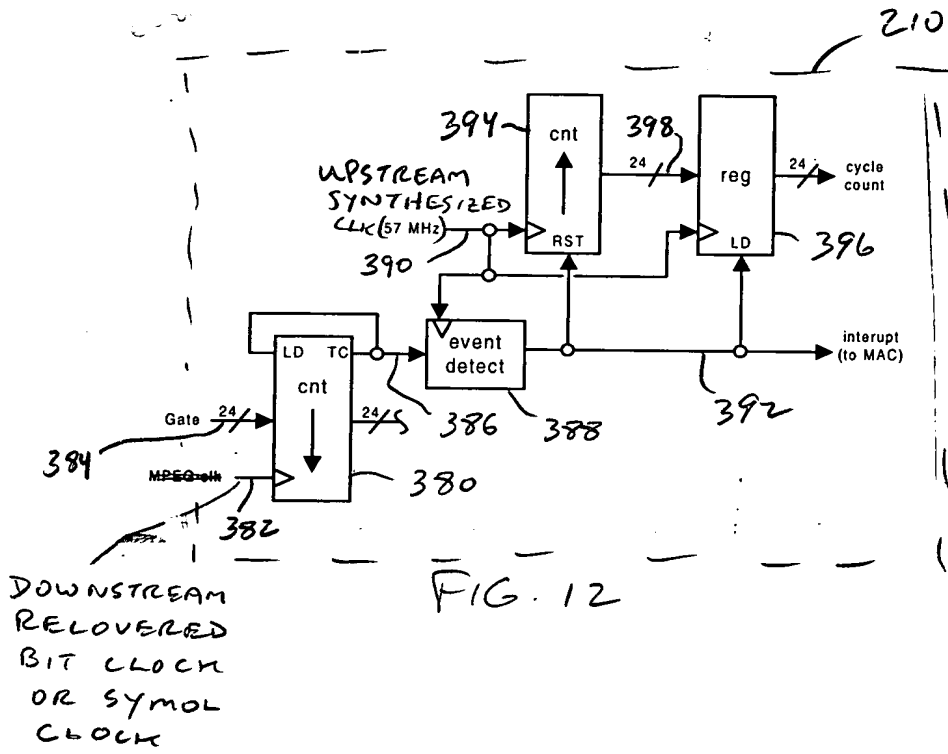


FIG. 12

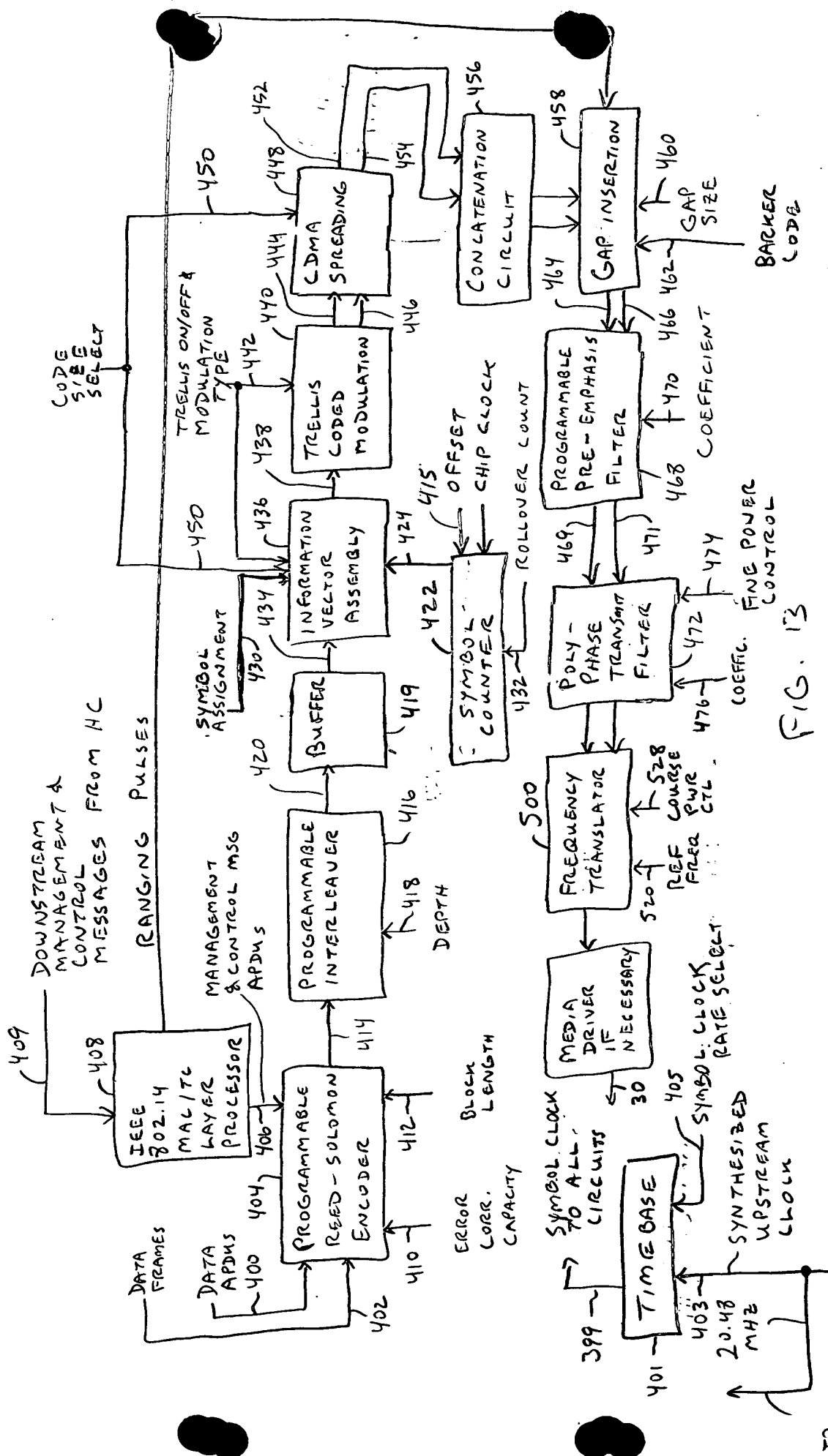
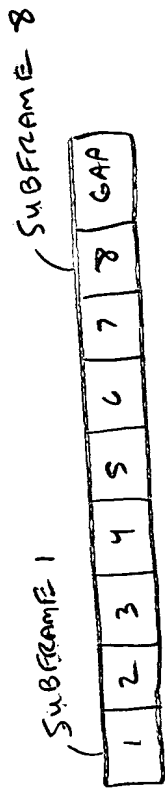
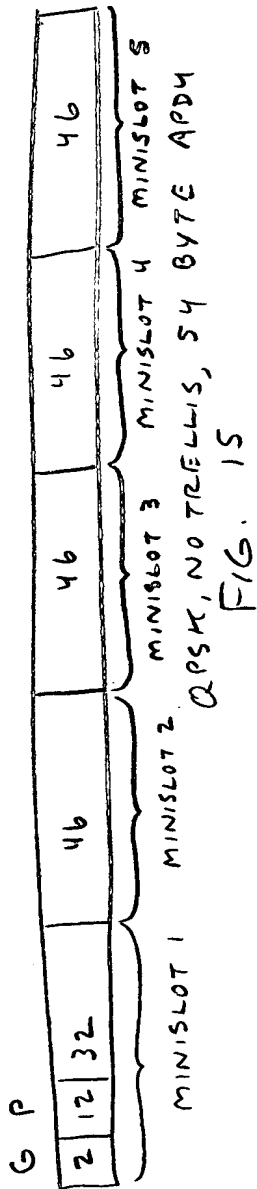
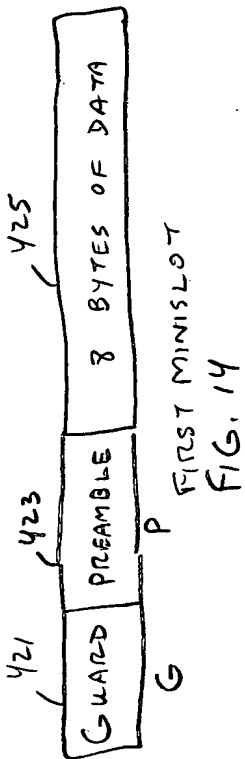
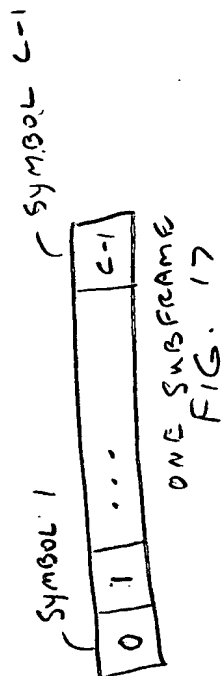


Fig. 13

TO
CIRCUITS
THAT NEED
THE MASTER
CLOCK TICK
RATE



ONE HS-CDMA FRAME
FIG. 16



ONLY CODES
1 & 2 ASSIGNED
FOR MINISLOT
IN WHICH THIS
SYMBOL WILL
BE SENT

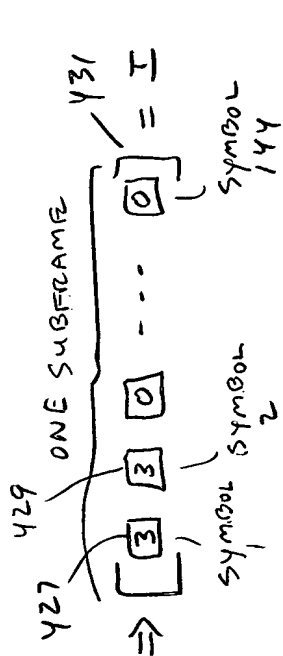


FIG. 13A: CREATE INFORMATION VECTOR = ONE SYMBOL

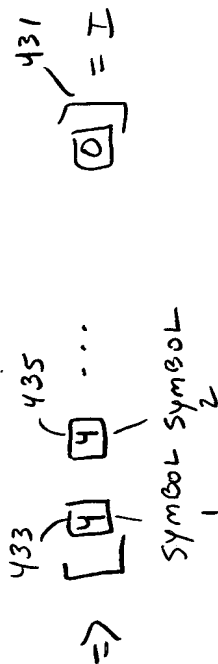


Fig. 18B

TRELLIS ENCODE
INFORMATION VECTOR

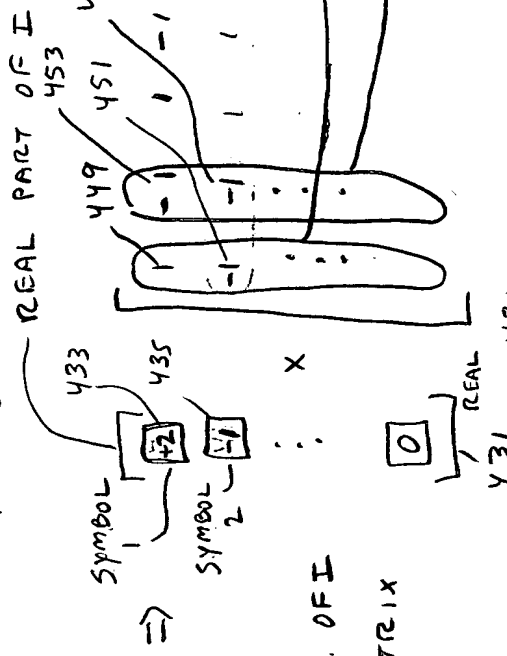
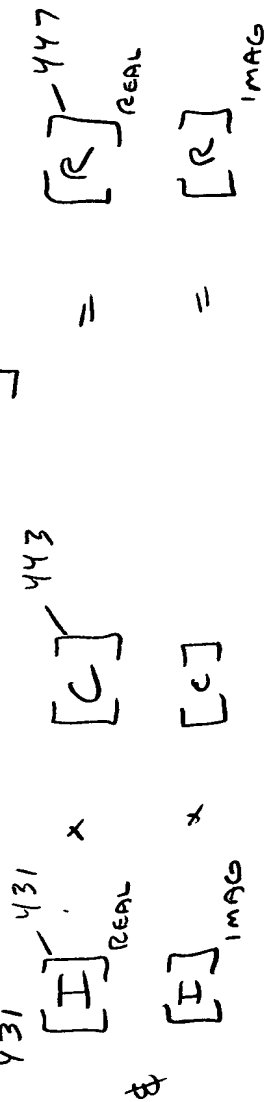


Fig. 18c

SPREAD SPECTRUM
OF TRELLIS
ENCODED INFOR-
MATION VECTOR
BY MATRIX MULT. OF 1
TIMES CODE MATRIX



POLYPHASE TRANSMIT FILTER

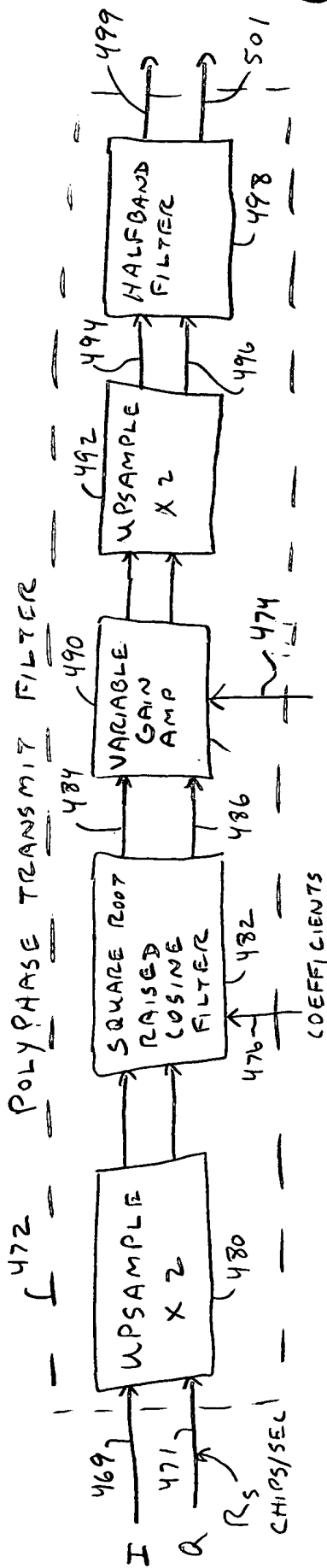


FIG. 19

COEFFICIENTS

FINE POWER CONTROL

499 I $[1, 0, -1, 0]$ ← QAM MODULATOR

502 510 506

Q 504 SUM 512 514

501 Q $[0, 1, 0, -1]$ 4 · R_s 508 REAL ONLY

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

504 510 506

FIG. 20

500

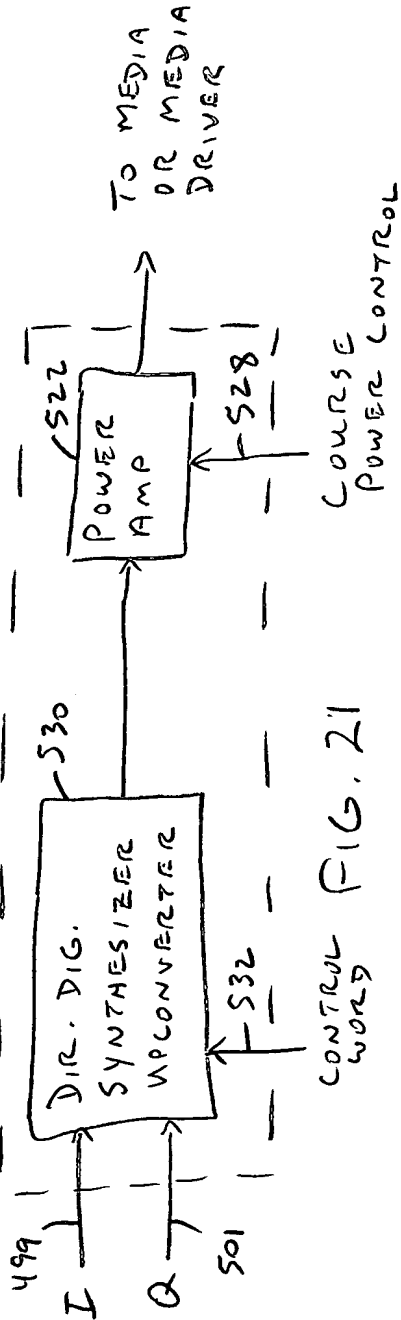


FIG. 21

COARSE POWER CONTROL

TO MEDIA OR MEDIA DRIVER

TO MEDIA OR MEDIA DRIVER

TO MEDIA OR MEDIA DRIVER

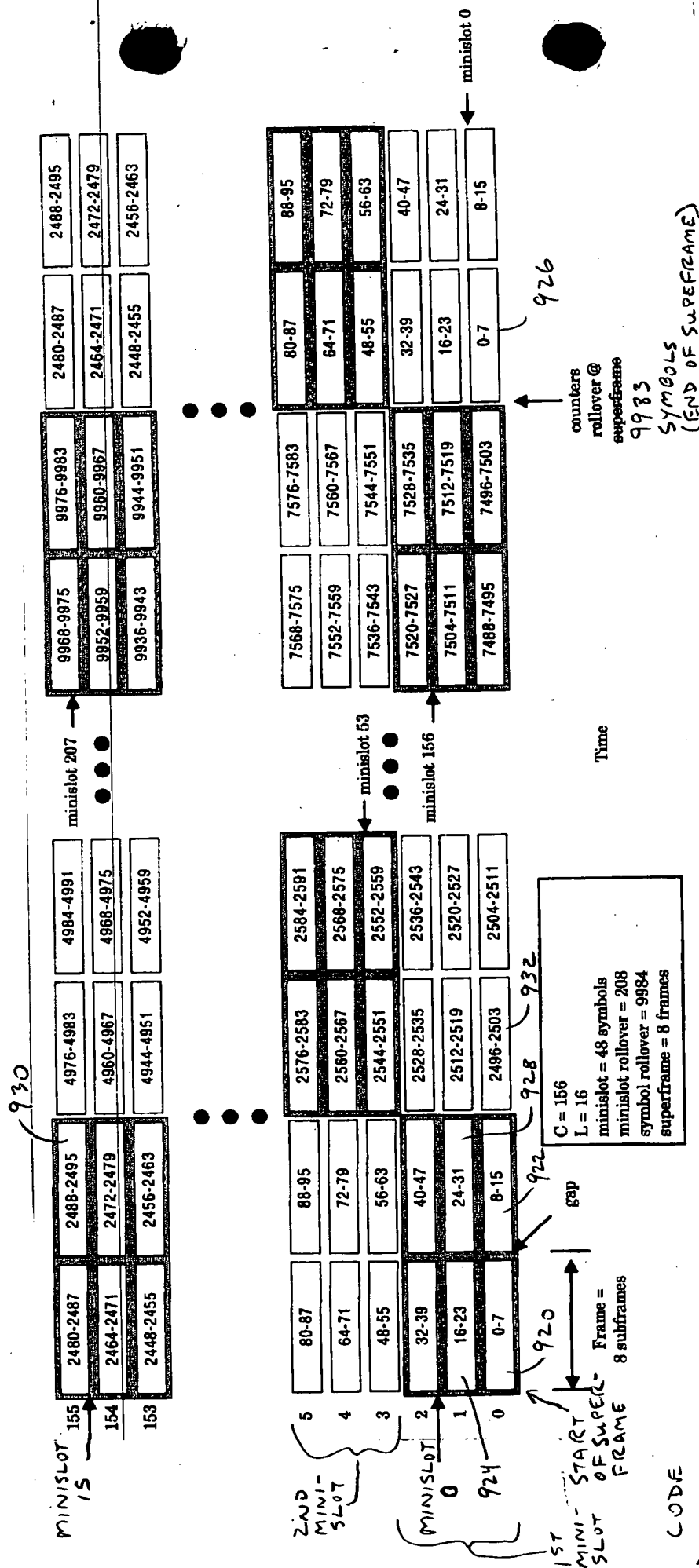


FIG. 22

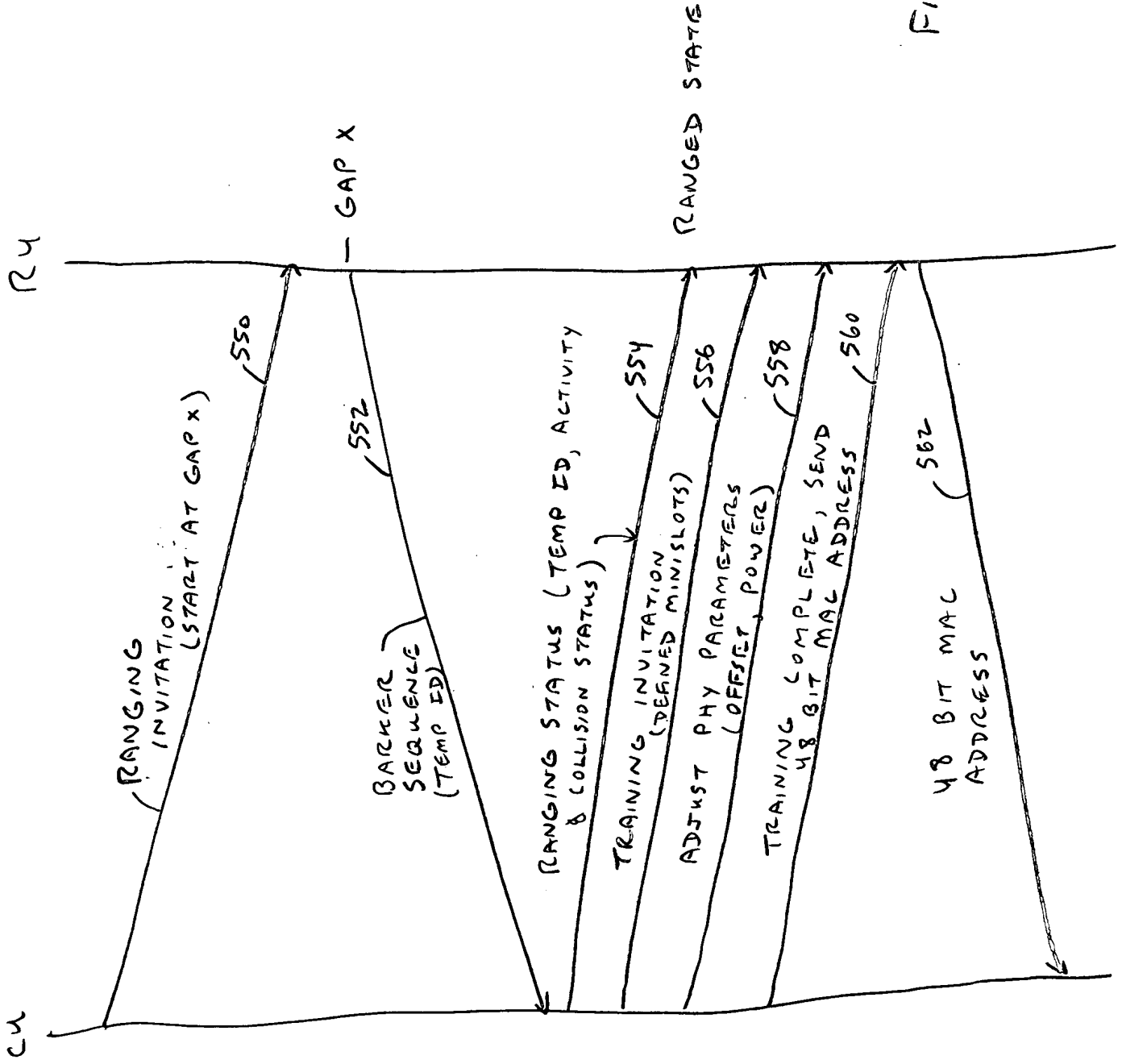
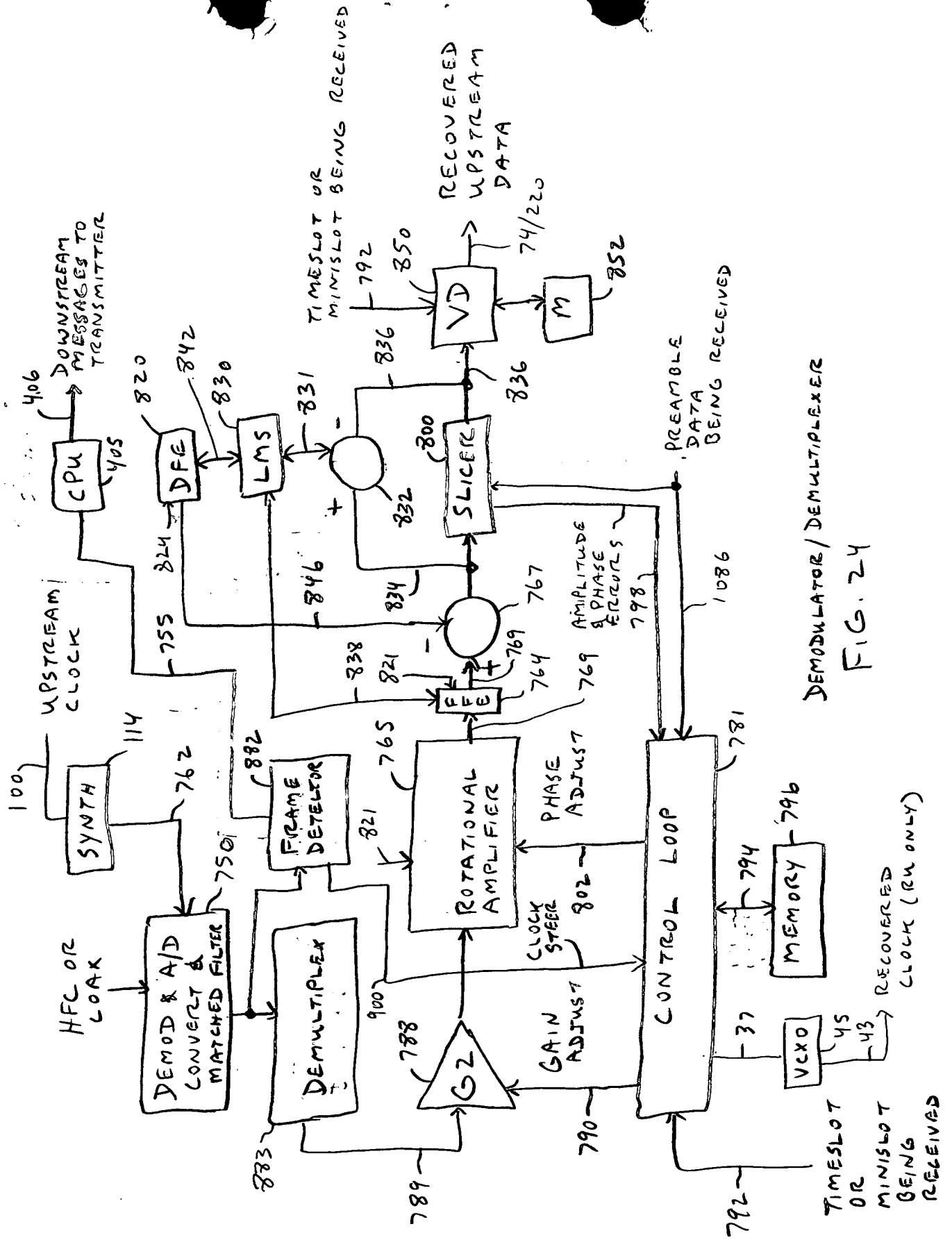


FIG. 23



DEMOMULATOR/DEMULTIPLEXER

FIG. 24